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PROGRAMMABLE HIGH RESOLUTION CHARACTER GENERATOR FOR VDU-K

(PROPOSED)

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PROGRAMMABLE HIGH RESOLUTION CHARACTER GENERATOR FOR VDU-K

PREFACE

This note describes a proposed method of providing a programmable high resolution character generator for the VDU-K card, used in the Interak 1 system.

It is not yet scheduled for production but these notes are being released for distribution to any people who express an interest in the subject, so that they may, if the wish, conduct their own experiments along broadly similar lines.

ISSUE 0 MANUAL PROGRAMMABLE HIGH RESOLUTION CHARACTER GENERATOR FOR VDU-K

CONTENTS

ERRATA

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General Features

* Power on default to standard VDU-K format - no need for any software changes.

* Electrically the PCG card becomes the "applications character set EPROM" for the VDU-K.

* Permits the existing 128 standard (or user-defined) characters of the VDU-K to be retained, and provides for an additional 128 completely programmable high resolution graphics or alphanumeric characters.

* Only 2K of additional system address space is required (Address F800h-FFFFh in the Interak 1 system)

* Effective resolution is 256 pixels horizontal by 240 pixels vertical = 61,440 pixels. (A programmable screen area 128 x 8 x 10 = 10,240 is available at any one time, which can be disposed in user-defined locations on the screen.)

* VDU-K text RAM still selects characters, so once high resolution characters have been defined they can be moved or copied on the screen at high speed by rewriting the VDU-K text RAM.

Introduction

It is assumed that the reader has a detailed working knowledge of the VDU-K card, and in particular is familiar with the way the pattern of bits in the EPROM character generator is turned into a display on the screen. Also it is assumed that the VDU-K is installed as part of an Interak 1 Computer system. This latter assumption lets the author quote actual addresses in the description which follows.

Each of the two possible 2K EPROM character generators on the VDU-K card contains the patterns for 128 characters, and so a grand total of 256 characters may be programmed into a pair of 2K EPROMs. (This is ignoring the VDU-K option whereby a 4K EPROM can be used in one socket, instead of the 2 x 2K EPROMs, one in each of the two sockets.)

If the user has the total amount of EPROM installed, and disables the "high bit invert" option, then when the following program in ZYBASIC is run, the whole character set can be observed on the screen, 3 times in all:

```
10   FOR J = #F000 TO #F2FF
20   POKE J,J
30   NEXT J
```

The addresses #F000 to #F2FF are the locations of the VDU text RAM in the memory map (the "#" prefix indicating hexadecimal notation in this manual). Like all the memory locations in an Interak 1 computer, only a single 8-bit byte can be contained in each, so the effect of line 20 (POKEing for example location #F000 with data #F000 will in fact only result in the location receiving #..00, the #F0.. having been lost since there was no space to receive it).

In other words, if you run the above program what you will see on the screen will be the character which corresponds to code #00, then #01, #02, and so on up to #FF. The character after #FF will simply be a repeat of #00. There are potentially 256 different characters, but they are bound to repeat when they are displayed in ascending sequence on the VDU-K screen, since the VDU-K can display 256 x 3 = 768 characters (#2FF in hex.) in all, and there are only 256 characters available for display.

As each character is made up of a matrix of 80 pixels ("pixel" = picture element, i.e. the smallest displayable entity) 8 horizontally by 10 vertically, then the resolution of the entire screen is 8 x 32 = 256 pixels horizontally, and 10 x 24 = 240 pixels vertically, i.e. 61,440 in all, which can be described as high resolution (although it should be noted that there is a trend nowadays that whenever the resolution of the screen is mentioned this also implies that the individual pixels are programmable; there is a clear need for a term which can be used to describe the resolution of a display without this sometimes ambiguous connotation).

For example, using the coarse set of block graphics characters contained in the standard VDU-K character generator, the size of each pixel which can be changed under program control is one quarter of the

size of each character cell, i.e. the resolution of the display which can be used to build up pictures using these pixels is 64 horizontally by 48 vertically, =3072. (The resolution can be increased by subdividing the character cell further making the programmable pixels smaller, but there is a limit to how much this can be done, before running out of space in the character generators.)

It can be seen that the only problem with the idea of having character generators in EPROM is that the characters they contain cannot be altered. The VDU-K manual divides the 256 characters into two 128-character classifications: the "standard" characters, and the "applications" characters. The "standard" character set includes all of the characters which are likely to be used fairly often by everyone, e.g. the upper and lower case letters, the numerals and punctuation signs, line drawing characters, and block graphic pixels; the "applications" characters are undefined and depend usually on the user's precise application.

It is in practice quite sensible and convenient to have the standard characters in EPROM, so that they are always there, and the software in the system is thus relieved of the overhead of carrying round a character set within its structure, but it is not so desirable to have the applications characters in EPROM (although it is cheap, which is an important point, since the VDU-K is a card which is often purchased in the very early stages by customers working to modest budgets).

The advantages of a RAM-based character generator are, it is hoped, obvious.

With many modern "home" computers undue emphasis is placed on "specmanship" (i.e. striving to achieve a specification which appears on paper superior to other similar comuters) and disregarding totally any question of whether or not this gives any practical performance benefits when the user comes to write his own programs. The twin penalties which are usually suffered when programmable high resolution graphics are dragged in simply to "sell" a computer, are either erosion of the user's memory space, as more and more of the system RAM is taken for the screen, and/or very much reduced speed of operation if the screen RAM is separated out independently from the user's RAM, thus requiring extensive port switching or other techniques to read and write to the screen memory.

The unreasoning attraction of fully programmable high resolution graphics for home computers regardless of the question of how difficult they may be able to use (as opposed to demonstrate) in practice, often makes the designers of such systems abandon the traditional (VDU-K style) architecture of having a Video Text RAM containsing ASCII codes which identify the appropriate character from a character generator.

It should therefore be remembered that this established method has some outstanding advantages. In the case of the standard VDU-K the single action of writing say the ASCII hex. code #41 to location #F000 will result in the complete letter 'A' appearing on the screen, i.e. a total of 80 pixels, since the 'A' is contained in an 8 x 10 pixel

matrix. If the method used for high resolution does not incorporate this character mapping technique then the same results have to be achieved in a much more laborious manner. For instance to display a letter 'A' on the screen given the ASCII hex. data #41, a tedious procedure of using a look up table has to be followed to get the required pattern of 10 bytes (80 pixels), and they have to be written to the screen as a sequence of 10 individual accesses. (This isn't so bad if they are in ten adjacent locations, as in this system, but it is much more tedious if the usual high resolution screen mapping is used where adjacent bytes are displayed continuously horizontally rather than grouped vertically.)

The problems which beset users of such systems are intensified when it is required that a program examine the screen to see what letter (if any) is displayed at a particular location. For example it might be required in a program to test and see if a letter 'A', or chessman, or whatever, is present on the screen at a particular location. With the VDU-K it is a simple matter of reading the text RAM, e.g. location #F000 used in the example above, to see if it contains say hex. #41, and is therefore an ASCII 'A'. With some current machines the problem is a nightmare: imagine the difficulty and time taken in being presented with a pattern of 80 dots at various locations on the high resolution screen, and being asked whether it is an 'A' or not, and if it is having to set a register to #41.

The above problems are not present in this design; the VDU-K text RAM is retained and can be written to and interrogated as before. Only the precise shape and form of the characters is altered, but each 80-pixel character block can still be selected by a single 1-byte access to the video text RAM if desired.

It is desirable that microprocessor can read the RAM-based character generator, which saves the wastage of memory and processing time if it was write-only, and a copy of the characters thus had to be kept somewhere else, in the user's RAM.

<u>Summary</u>

High resolution programmable graphics characters are added to the VDU-K by incorporating a circuit board which takes the place electrically of the optional 2K "applications" character generator EPROM.

The PCG card also physically takes the place of the EPROM, because the connection is made by a piece of ribbon cable, terminated in a 24-pin header, plugged into the "applications" EPROM socket.

Except for the ribbon cable, the graphics card plugs into the bus in the same way as the other cards, and appears simply as read/write memory at location #F800-#FFFF.

The VDU-K will in consequence behave exactly as it did before, except that now the applications characters will depend on the contents of the RAM on the PCG card instead of those of a pre-programmed EPROM.

Since the VDU-K text RAM is still operational, once high resolution characters have been defined they can be used elswhere on the screen by using the same code. This saves the laborious task of copying the individual pixels to the new location; all the eighty dots which make up a character can be copied at a stroke by using the same code elsewhere on the screen.

Design Goals

The "no snow" circuitry of the VDU-K has been adopted for this design. It has not been tested, but if it works this will mean that the data held in the RAM character generator can altered even while it is in use, without disturbing the display.

The whole circuitry has to fit on a single card.

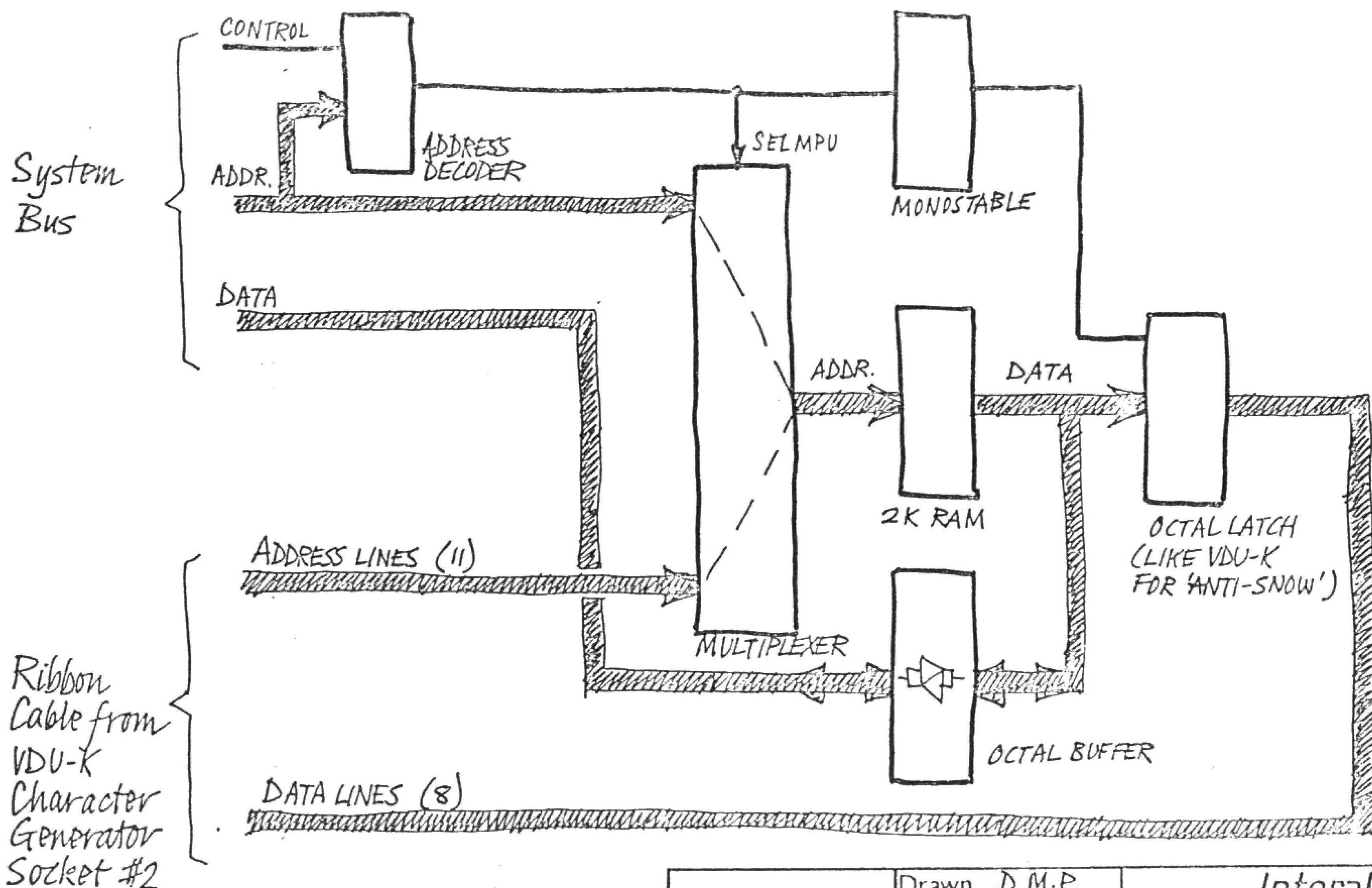
Bus loading to be kept to a minimum. (Due to shortage of space on the card for buffering, and timing requirements, some lines may have up to three LS loads rather than the single LS load desired.)

Circuit Diagrams

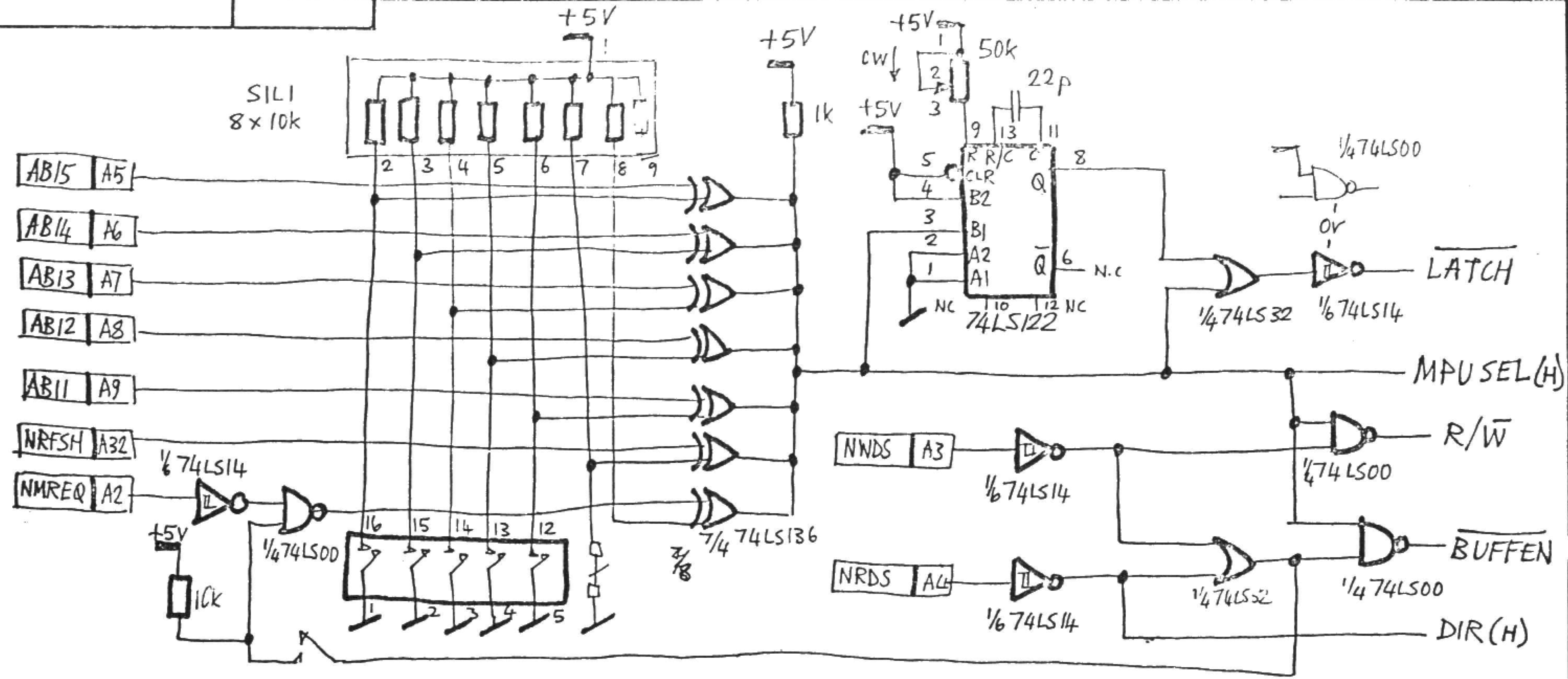
The following diagrams are, it should be stressed, only rough preliminary ideas; they have not been checked, nor tested, and consequently should not yet be used for anything more than guidance for the user's own experiments.

Use of 6116

The choice of a single 6116 2K x 8 CMOS Static RAM rather than the equivalent 4 x 2114Ls is fairly obvious. The experimenter should be warned however that the 6116 may cause some initial problems. As the 6116 is very fast and has slightly different timing requirements to the 2114L it can often be more susceptable to "noise" and other switching transients. It is anticipated that the 2114L type of RAM would not give any similar trouble here, but users of the 6116 in this type of circuit should remember these potential difficulties. (The experience to make these comments was gained during the design of the VDU-K, when the old fashioned 2114L was used reluctantly in the end in place of the newer 6116, because of its more forgiving ways when subjected to abuse in its operating conditions.)



Drawn D.M.P.	Interak
Date 8-2-83	X PCG-1 PROGRAMMABLE CHARACTER GENERATOR BLOCK DIAG
Scale –	1

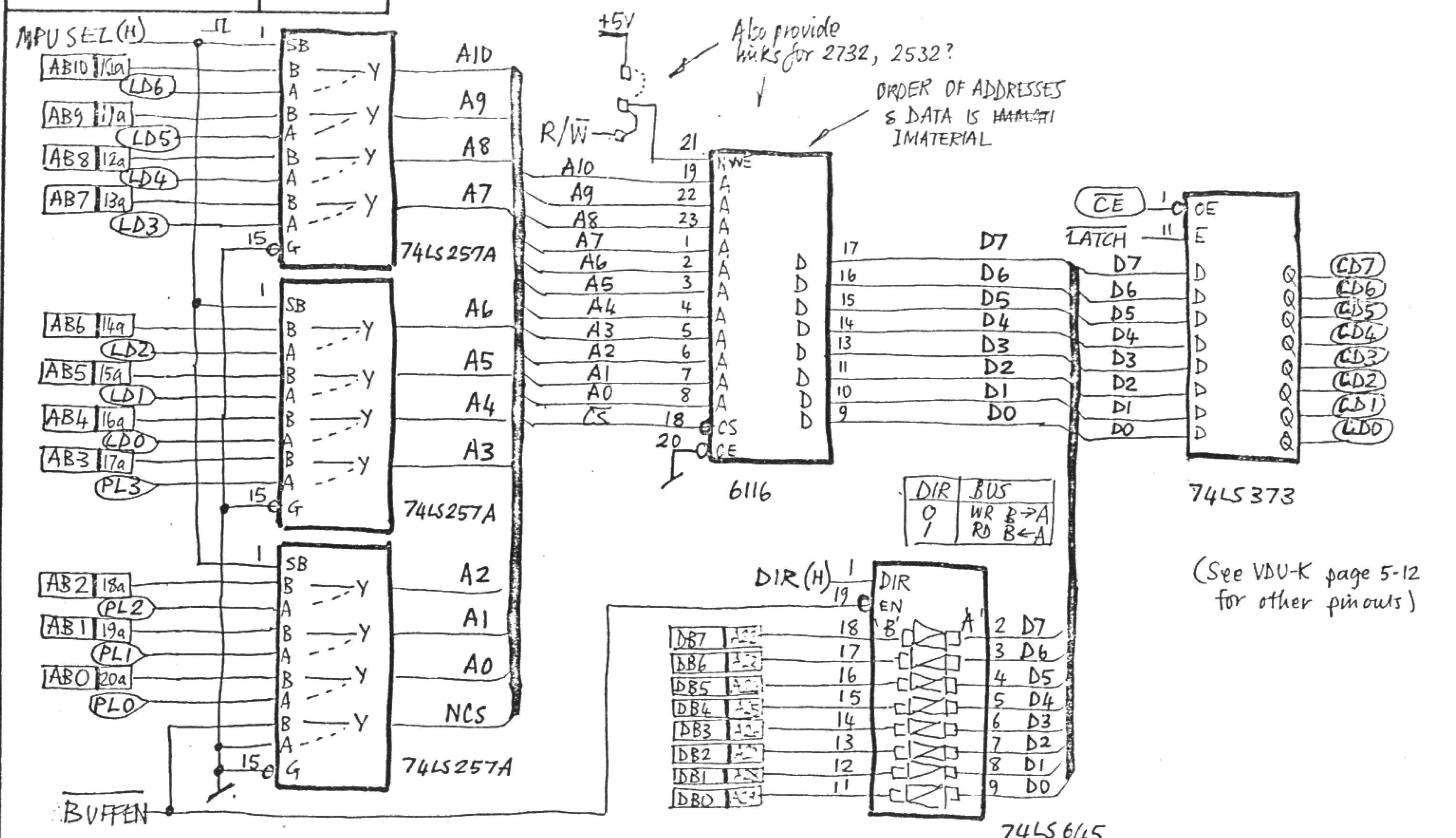


Drawn	D.M.P.
Date	7-11-82
Scale	-

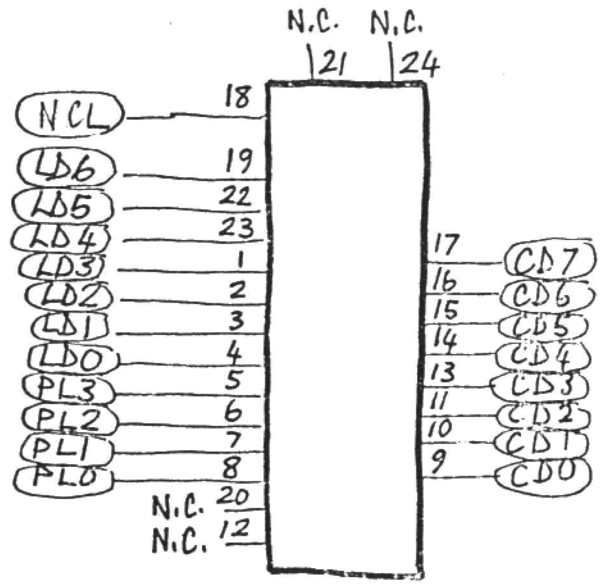
Greenbank Electronics

XPCG-1 CIRCUIT DIAGRAM

2



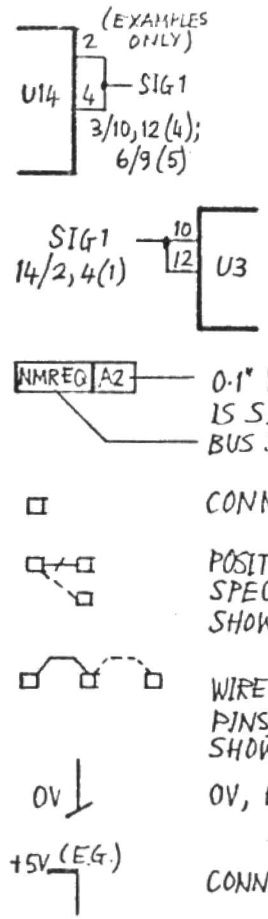
Drawn DMP	**Greenbank Electronics**	
Date 7-11-82	XPCG-1 CIRCUIT DIAGRAM	
Scale -		3



24-pin Ribbon Cable header
connection to VDU-K
(Both ends terminated identically)

Drawn	D.M.P.	**Greenbank Electronics**
Date	7-11-82	X PCG-1 CIRCUIT DIAGRAM
Scale	–	
		4

KEY TO SYMBOLS USED ON CIRCUIT DIAGRAMS



OUTPUT PINS 2 AND 4 OF U14 PRODUCE A SIGNAL CALLED SIG1, WHICH IS CONNECTED TO U3 PINS 10, 12 (SHEET 4); AND U6 PIN 9 (SHEET 5).

INPUT PINS 10 AND 12 OF U3 RECEIVE A SIGNAL CALLED SIG1 WHOSE SOURCE IS U14 PINS 2,4 (SHEET 1).

0·1" PITCH EDGE CONNECTOR POSITION E.G. A2 IS SIDE A, PIN 2; B3 IS SIDE B PIN 3, ETC.
BUS SIGNAL NAME.

CONNECTION PAD OR PIN.

POSITION WHERE TRACK MAY BE CUT FOR SOME SPECIAL PURPOSE; ALTERNATIVE CONNECTION SHOWN DOTTED.

WIRE LINK (EG. WIRE WRAPPED TO TERMINAL PINS) SHOWN SOLID. ALTERNATIVE POSITION SHOWN DOTTED.

0V, EARTH CONNECTION.

CONNECTION TO NAMED POWER SUPPLY RAIL.

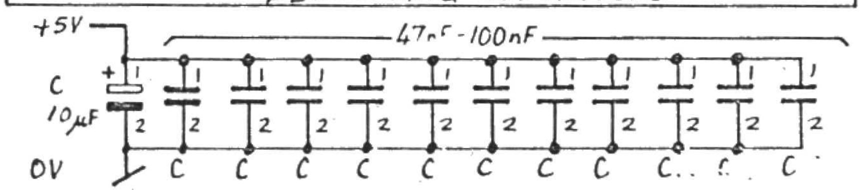
POWER SUPPLIES

(EDGE CONNECTOR PINS A37, B37 REMOVED FOR POLARISING KEY)

+12V	A35	+12V	B35	+12V	+12V NOT USED ON THIS CARD.
+12V	A36	+12V	B36		
−12V	A38	−12V	B38	−12V	−12V NOT USED ON THIS CARD.
−12V	A39	−12V	B39		
0V, E	A40	0V, E	B40	0V	0V, EARTH POWER RAIL.
0V, E	A41	0V, E	B41		
+5V	A42	+5V	B42	+5V	+5V POWER RAIL.
+5V	A43	+5V	B43		

IC POWER SUPPLY CONNECTIONS ARE LISTED IN A TABLE IN ONE CORNER OF EACH SHEET OF THE MAIN CIRCUIT DIAGRAMS. FOR CLARITY OF LOGIC FLOW THE POWER SUPPLY CONNECTIONS ARE NOT NORMALLY INCLUDED ON THE GRAPHIC PART OF THE CIRCUIT DIAGRAMS. CONNECTIONS TO THE POWER SUPPLY RAILS FOR OTHER PURPOSES (E.G. ENABLES, DISABLES ETC.) ARE SHOWN.

DECOUPLING CAPACITORS



Drawn	D.M.P.
Date	8.2.83
Scale	-

Interak

XPCG-1 CIRCUIT DIAGRAM, SHEETS : KEY TO SYMBOLS, AND POWER SUPPLIES

OF

COMPONENT PRICE LIST FOR XPCG-1 CARD — List Ref: XPCG-1/P3

(Prices exclude VAT) — February 1983, Revised July 1985

Prices each, ex. VAT

Resistors 0.25W						
CR251K0	1	XR		0.02	0.02	
CR2510K	1	XR		0.02	0.02	
SIL Resistor (Use Socket)						
8x10K	1	XSIL1 (9 pin)		0.26	0.26	
Variable Resistor (Multiturn)						
MULTI50K	1	XRV1		0.78	0.78	
	4		Resistor Pack XPCG1		1.08	1.08
Capacitors						
("CER" = Ceramic; "DEC" = 47n - 100n Decoupling grade polyester, or Ceramic; "MAL" = Low Leakage Miniature Aluminium Electrolytic)						
CER22P 5%	1	XC		0.05	0.05	
DEC	5	XC		0.09	0.45	
MAL10U	1	XC		0.07	0.07	
	7		Capacitor Pack CXPCG1		0.57	0.57
Integrated Circuits (Use Sockets)						
6116	1	XU	(24 pin)	4.75	4.75	
74LS00	1	XU	(14 pin)	0.36	0.36	
74LS14	1	XU	(14 pin)	0.49	0.49	
74LS32	1	XU	(14 pin)	0.36	0.36	
74LS122	1	XU	(14 pin)	0.98	0.98	
74LS136	2	XU	(14 pin)	0.41	0.82	
74LS257(A)	3	XU	(16 pin)	0.56	1.68	
74LS373	1	XU	(20 pin)	1.08	1.08	
74LS645	1	XU	(20 pin)	1.52	1.52	
	12		Integrated Circuit Pack ICXPCG1		12.04	12.04
DIL Switch						
DILSW8	1	XS1	(16 pin)	1.50	1.50	
			DIL Switch Pack SWXPCG1			1.50
DIL & SIL Sockets						
9SCON	1	XSIL1		0.06	0.06	
DIL14	6	XU		0.10	0.60	
DIL16	4	XS1; XU		0.10	0.40	
DIL20	1	XU		0.22	0.22	
DIL24	2	XU		0.25	0.50	
	14		DIL & SIL Socket Pack SKXPCG1		1.78	1.78
0.1" Pitch Pin Assemblies						
PINASY3	1	P1		0.11	0.11	
			Pin Assembly Pack PNXPCG1		0.11	0.11
Sundry						
JLINK			1 off	0.20	0.20	
Pre-stripped Insulated Wire for links:						
PSW25		(including some spares)	3 off	0.01	0.03	
	4		Sundry Pack SYXPCG1		0.23	0.23
			Total cost of kit of all parts listed so far: PXPCG1			17.31

Options etc., see next page.

OPTIONS (i.e. Items not included in standard kit of parts)

Prices each, ex. VAT

Prototyping card type DIP-1 (no XPCG-1 card planned at present)	BDIP1	10.95	
Notes on XPRN-2 (Zero rated for VAT)	MXPCG1	1.00	0%
1" Card Front Kit, inc fixings and mtg. brackets, new type	CF1	2.99	
ditto, old (RS) type	OCF1	3.99	
24-pin header to 24-pin header ribbon cable (approx 330 mm)	PCGLD1	4.25	

Add 50p handling charge to each transaction, and 15% VAT.

Greenbank Electronics,
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New Ferry, Wirral,
Merseyside. L62 5AG

Telephone:- 051-645 3391

Access/Visa Welcome (no surcharges).